

Bhoj Reddy Engineering College for Women: Hyderabad

Department of Electronics and Communication Engineering

Lesson plan of faculty member for the academic year 2016–17

Class: II B Tech

Branch-Section: ECE-C

Semester: II

Subject: Digital Design using Verilog HDL (DDV)

Lectures per week: 4+1 (Tutorial)

Lecture Number	Topics to be covered	Date(s)
UNIT - I: Introduction		
1.	Introduction to Verilog	9 December16
2.	Verilog as HDL, Levels of design Description	10 December16
3.	Tutorial (G3, G1, G2):	----, ----, 10 December16
4.	Concurrency, Simulation and Synthesis	13 December 16
5.	Functional Verification	14 December 16
6.	Module, Simulation and Synthesis Tools, Test Benches	16 December 16
7.	Language constructs and conventions: Introduction	17 December 16
8.	Tutorial (G3, G1, G2): System Tasks, Programming Language Interface (PLI)	13, 14 and17 December 16
9.	Keywords, Identifiers	20 December 16
10.	White Space Characters, Comments, Numbers	21 December 16
11.	Strings, Logic Values, Strengths	23 December 16
12.	Data Types, Scalars and Vectors	24 December 16
13.	Tutorial (G3, G1, G2): Related examples, programs.	20, 21 and 24 December 16
14.	Parameters, Operators	27 December 16
15.	AND Gate Primitive, Module Structure	28 December 16
16.	Other Gate Primitives	30 December 16
17.	Illustrative Examples, Tri-State Gates	31 December 16
18.	Tutorial (G3, G1, G2): Exercises.	27, 28 and 31 December 16
19.	Array of instances of primitives	3 January17
UNIT- II: Gate Level Modeling		
20.	Design of Flip – Flops with gate primitives	4 January 17
21.	Delays, Strengths	6 January 17
22.	Construction Resolution	7 January 17
23.	Tutorial (G3, G1, G2): Exercises.	3, 4 and 7 January 17
24.	Net Types, Design of Basic Circuits	10 January 17
25.	Modeling at Dataflow level	11 January 17
26.	Continuous Assignment Structure	13 January 17
27.	Tutorial (G3, G1): Exercises.	10, 11 and __ January 17
28.	Delays & Continuous Assignments	17 January 17
29.	Operations and Assignments	18 January 17
30.	Functional Bifurcation	20 January 17
31.	Initial Construct, Always Construct, Examples	21 January 17
32.	Tutorial (G2, G3, G1): Assignment to vectors, operators	17,18 and 21 January 17
33.	Assignments with Delays, Wait Construct	24 January 17
UNIT- III: Behavioral Modeling		
34.	Designs at Behavioral Level	25 January 17

35.	Blocking and Non-Blocking Assignments	27 January 17
36.	Tutorial (G3, G1, G2): Multiple Always Blocks	9, 10 and 14 February17
37.	The case statement, Simulation Flow if and if-else constructs	21 February 17
38.	assign – deassign construct, repeat construct	22 February 17
39.	for loop, Disable construct	25 February 15
40.	Tutorial (G3, G1, G2):	21, 22 and 25 February 17
41.	while loop, forever loop	28 February 17
42.	Delays, Strengths	1 March 17
43.	parallel blocks, force-release construct	3 March 17
44.	Event.	4 March 17
45.	Tutorial (G3, G1, G2): Array of Instances of Primitives,	28 February, 1 and 4 March 17
46.	Switch level modeling: Introduction	7 March 17
47.	Basic Transistor Switches, CMOS Switch	8 March 17
48.	Bi – directional Gates	10 March 17
49.	Time Delays with Switch Primitives	11 March 17
50.	Tutorial (G3, G1, G2): Exercises.	7, 8 and 11 March 17
51.	Strength Contention with Trireg Nets, exercises.	14 March 17
UNIT-IV: Switch Level Modelling		
52.	System tasks, functions	15 March 17
53.	compiler directives	17 March 17
54.	Hierarchical Access, user defined primitives	18 March 17
55.	Tutorial (G3, G1, G2): Instantiations with Strengths and Delays	14,15 and 18 March 17
56.	Sequential Circuit Description	21 March 17
57.	Sequential models- feedback model	22 March 17
58.	Capacitive models	24 March 17
59.	Functional Register	25 March 17
60.	Tutorial (G3, G1, G2): Examples, Programs	21, 22 and 25 March 17
61.	Static Machine Coding	28 March 17
UNIT-V: Sequential Circuit Description		
62.	Sequential Synthesis	31 March 17
63.	Sequential circuit testing	1 April 17
64.	Tutorial (G3, G1, G2): Examples, Programs	28 March 17, -----,1 April 17
65.	Basic Memory components	4 April 17
66.	Design verification	7 April 17
67.	Assertion verification	8 April 17
68.	Tutorial (G3, G1, G2): Examples, Programs	4, ----, 8 April 17
69.	Test bench techniques	11 April 17
70.	Previous question papers discussion	12 April 17
71.	Tutorial (G3, G1, G2): Revision	11, 12 and ___ April 17

TEXT BOOKS:

1. T R. Padmanabhan, B Bala Tripura Sundari, Design through Verilog HDL, Wiley 2009
2. Zainalabdein Navabi, Verilog Digital system design, TMH ,2nd Edition
3. Verilog HDL- Samir Palnitkar,2nd Edition, Pearson Education, 2009

Name and signature of the faculty: S Manjula ----

Name and signature of Head of the Department: Ms N Shribala ----