Bhoj Reddy Engineering College for Women: Hyderabad

Department of Electronics and Communication Engineering

Lesson Plan of faculty member for the academic year 2015 – 2016

Name of the faculty member and Department : K.SRINIDHI REDDY , ECE

Subject: VLSI DESIGN (VLSI) Class: III B.Tech.

Branch & Section: ECE-A Semester: II

No. of lectures per week: 4+1 (Tutorial)

Lecture Number	Date/ month	Topic to be covered
	Unit I	**INTRODUCTION**
1.	7/12/15	Introduction to Syllabus, Basics of IC
2.	8/12/15	Introduction to IC Technology
3.	9/12/15	Oxidation, Lithography (Extra topic)
4.	9/12/15,10/12/15, 11/12/15	Tutorial(G1,G3,G2)Fundamentals of VLSI Technology
5.	11/12/15	Diffusion , Ion Implantation (Extra topic)
6.	14/12/15	Metallization, Encapsulation (Extra topic)
7.	15/12/15	Fabrication Process-MOS,PMOS
8.	16/12/15	NMOS ,CMOS
9.	16/12/15,17/12/15, 18/12/15	Tutorial(G1,G3,G2)Fabrication Steps
10.	18/12/15	BICMOS
		Basic Electrical Properties
11.	21/12/15	Basic Electrical Properties of MOS and BiCMOS circuits: Ids-Vds relationship
12.	22/12/15	MOS transistor threshold Voltage
13.	23/12/15	Gm, gds, figure of merit
14.	23/12/15	Tutorial(G1) Problems on Ids vs Vds
15.	28/12/15	Pass transistor
16.	29/12/15	NMOS Inverter
17.	30/12/15	Various pull-ups
18.	30/12/15,31/12/15, 01/01/16	Tutorial(G1,G3,G2) Problems on threshold voltage
19.	01/01/16	Various pull-ups(continued)

20.	04/01/16	CMOS inverter analysis and design
21.	05/01/16	BiCMOS inverter
	UNIT II	**VLSI CIRCUIT DESIGN PROCESS**
22.	06/01/16	VLSI design flow
23.	06/01/16,07/01/16, 08/01/16	Tutorial(G1,G3,G2) Problems on Rds,gm
24.	08/01/16	MOS layers
25.	11/01/16	Stick diagrams
26.	12/01/16	Design Rules and layout 2 micron
27.	13/01/16	CMOS design rules
28.	13/01/16	Tutorial(G1) Problems on logic gate implementation using pmos logic
29.	18/01/16	Design rules for wires, contacts and Transistor
30.	19/01/16	Layout using NMOS, CMOS AND GATES
31.	20/01/16	Scaling of MOS circuits
	UNIT III	**GATE LEVEL DESIGN**
32.	20/01/16,21/01/16, 22/01/16	Tutorial(G1,G3,G2) problems on Stick diagrams using nmos and pmos logic
33.	22/01/16	Logic gates and other complex gates , Switch Logic
34.	25/01/16	Alternate gate circuit, Basic circuit Component
35.	27/01/16	Sheet resistances , Area capacitance Units
36.	27/01/16,28/01/16, 29/01/16	Tutorial(G1,G3,G2) problems on Stick diagrams using nmos and pmos logic
37.	29/01/16	Calculations delays, Driving large capacitive loads
38.	22/02/16	Wiring Capacitance ,Fan in Fan out, Choice of layers
	Unit IV	**DATA PATH SUBSYSTEMS**
39.	22/02/16	SUBSYSTEM DESIGN
40.	23/02/16	Shifters
41.	24/02/16	Adders
42.	24/02/16,25/02/16, 26/02/16	Tutorial(G1,G3,G2) problems on layout diagrams using cmos logic
43.	26/02/16	Adders(cont..)
44.	29/02/16	ALU'S

45.	01/03/16	Multipliers
46.	02/03/16	Parity generators
47.	02/03/16,03/03/16, 04/03/16	Tutorial (G1,G3,G2) problems on Sheet resistance Rs and inverter ON resistance Ron
48.	04/03/16	Comparator
49.	08/03/16	Zero /One detector
50.	09/03/16	Counters
		ARRAY SUBSYSTEMS
51.	09/03/16,10/03/16, 11/03/16	Tutorial(G1,G3,G2) problems on adders, Shifters
52.	11/03/16	SRAM
53.	14/03/16	DRAM
54.	15/03/16	ROM
55.	16/03/16	Serial Access Memories
56.	16/03/16,17/03/16, 18/03/16	Tutorial(G1,G3,G2) problems on Counters
57.	18/03/16	Content Addressable Memory
	UNIT V	**SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN**
58.	21/03/16	PLA
59.	22/03/16	FPGA, CPLD
60.	24/03/16	Tutorial(G3) Problems on PAL
61.	28/03/16	Standard cells ,PAL
62.	29/03/16	Design Approach
63.	30/03/16	Parameters influencing low power design
		CMOS TESTING
64.	30/03/16,31/03/16, 01/04/16	Tutorial(G1,G3,G2) Problems on PROM
65.	01/04/16	Need for testing
66.	04/04/16	Test Principles
67.	06/04/16	Design Strategies for test
68.	06/04/16,07/04/16	Tutorial(G1,G3) problems on PLA and LUT
69.	11/04/16	Chip level test Technique

70.	12/04/16	System Level Test technique
71.	13/04/16	Layout Design for improved testability
72.	13/04/16	Tutorial (G1) problems on stuck at faults

TEXT BOOKS:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI,2005 Edition.
2. VLSI Design- K.Lal Kishore.V.S.V.Prabhakar, I.K.International, 2009.
3. CMOS VLSI Design – Niel H.E.Weste, David Harris, Pearson, 2009.

REFERENCE BOOKS:

1. CMOS logic circuit design john p Uyemura, Springer, 2007.
2. Modern VLSI Design-Wayne Wolf Pearson education, 3rd edition, 1997.

Name : K. Srinidhi Reddy Signature of the faculty with date:

HoD Signature: